Logos2 SEU Application Guide

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Document version revision history

VERSION NUMBER	RELEASE DATE	REVISION HISTORY
V0.1	2019-10- 15	initial version

Explanation of terminology

ABBREVIATION	FULL SPELLING	ЗНАЧЕНИЕ НА РУССКОМ
SEU	Single Event Upsets	Расстройство единичного события
GTP	General Technology Primitive	Модели логических примитивов

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1. Overview

1.1 Introduction

This document mainly introduces how the Logos2 chip forms a complete SEU detection system by calling GTP_IPAL_E2 for user reference.

1.2 Main functions

The main functions supported by the system are as follows:

- Send data streams or configuration registers through the GTP parallel interface and read back registers or data.
- Read back CRC check data
- Complete SEU error detection and correction

1.3 Design information

(List the main resources used)

TBC .

1.4 Resource usage

(List the main resources used)

TBC .

2. SEU detection function description

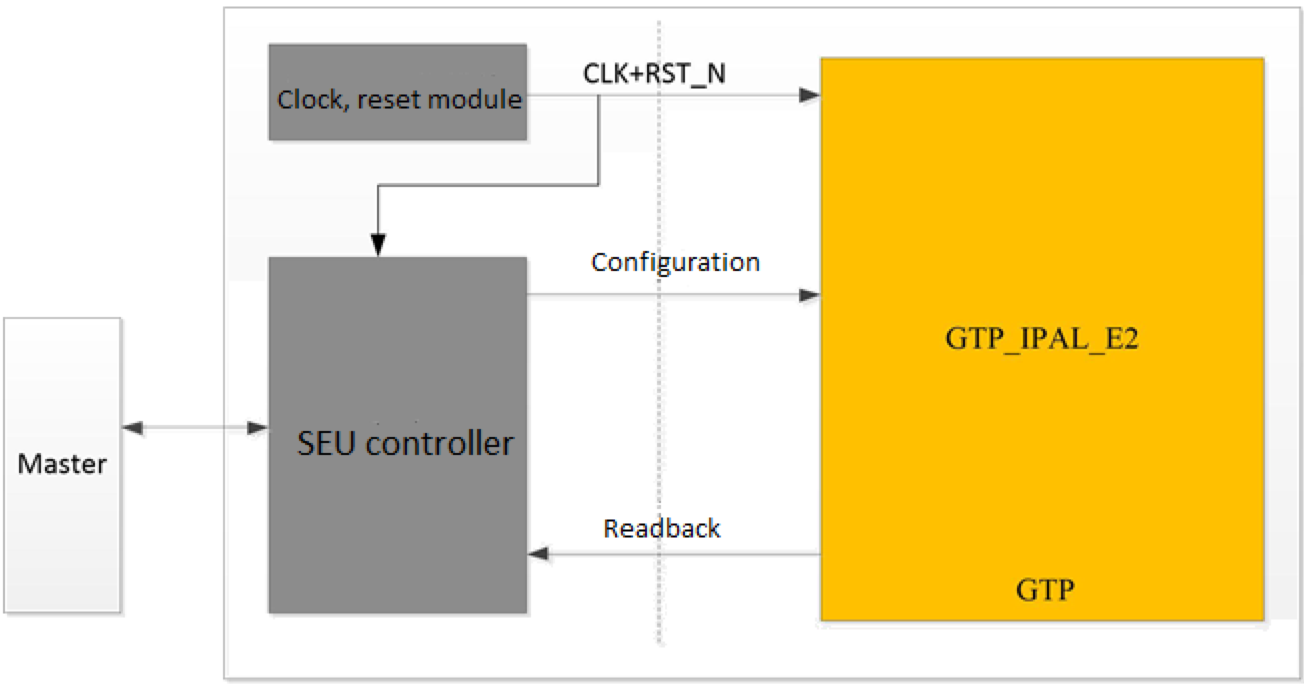


Figure 1 GTP_IPAL_E2 Application Introduction

Figure 1 shows an application block diagram of instantiating GTP_IPAL_E2 for SEU detection, which includes four parts: instantiated GTP_IPAL_E2, clock and reset module, SEU controller, and external master module.

GTP_IPAL_E2 inputs instructions or data through the parallel port to read and write the corresponding configuration register. Or write and read back the data of a certain frame of a certain column in a certain area in the configuration memory. Complete CRC detection or SEU detection on the data read back.

The clock and reset modules provide clock and reset signals for the GTP_IPAL_E2 module and the SEU controller module.

SEU controller is used to control streaming, configuration and readback, and communicates through the parallel interface of GTP_IPAL_E2. According to the SEU error detection and correction process, the data stream transmission and CRC readback as well as the readback and storage of ECC information and status are completed.

The external Master is used to control SEU detection startup and flow control.

The first step of applying GTP_IPAL_E2 for SEU detection is to perform the streaming operation first, and the second step will read back the CRC to determine whether the data is normal. If the data is normal, the third step of SEU inspection can be performed. If the data is abnormal, consider reconfiguring or terminating the operation.

2.1 Perform flow control

To complete streaming, configuration, and readback operations through the GTP_IPAL_E2 interface, you need to understand the timing and packet format of the GTP parallel interface.

The interface timing is illustrated in Figure 6 GTP_IPAL_E2 read and write interface timing. The following mainly introduces the packet format of the stream.

There are two types of data stream packets: type 1 and type 2. Type 1 packet is used for register reading and writing, and consists of a packet header part and a data part. The header of the type 1 packet is a 32-bit word, followed by data, and the data is in 32-bit words.

If the number of 32-bit words following the header specified in the header part is 0, then the packet has only the header part and no data part, and is an empty packet. The format of Type 1 header is as follows:

[31:29]	[28:27]	[26:22]	[21:0]
Header type	opcode	Register address	Number of 32-bit words
101	00: NOP 01:write 10:read 11:reserved	Register address	The number of 32-bit words following the header

Type 2 packets are used to read and write configuration memory. Type 2 packets consist of a header part and a data part. The header of the type 2 packet is a 32-bit word, followed by data, and the data is in units of 32-bit words.

Type 2 packets must follow type 1 empty packets. The type 2 packet does not specify the register address, and uses the address specified by the previous type 1 empty packet.

The format of Type 2 header is as follows:

[31:29]	[28:27]	[26:0]
Header type	opcode	32-bit words
010	00: NOP 01: Write 10: Read 11: Reserved	The number of 32-bit words following the header

2.2 CRC Read back process

The first step in applying GTP_IPAL_E2 for SEU inspection is to read back the CRC to determine whether the data is normal. If the data is normal, the second step of SEU inspection can be performed. If the data is abnormal, consider reconfiguring or terminating the operation.

Now we will introduce the detailed operation process of reading back the CRC in the first step:

Table 1 Read back CRC check process description

Send 100 fill words (32'hFFFFFFFF) bit stream	
Synchronize	
1	Write the SEU register to enable CRC readback and disable SEU error detection and correction.
2	Read back configuration memory
3	Write RRBCRC command to CMDR register
4	Read back configuration memory
5	Write RBCRC command to CMDR register
6	View readback CRC results

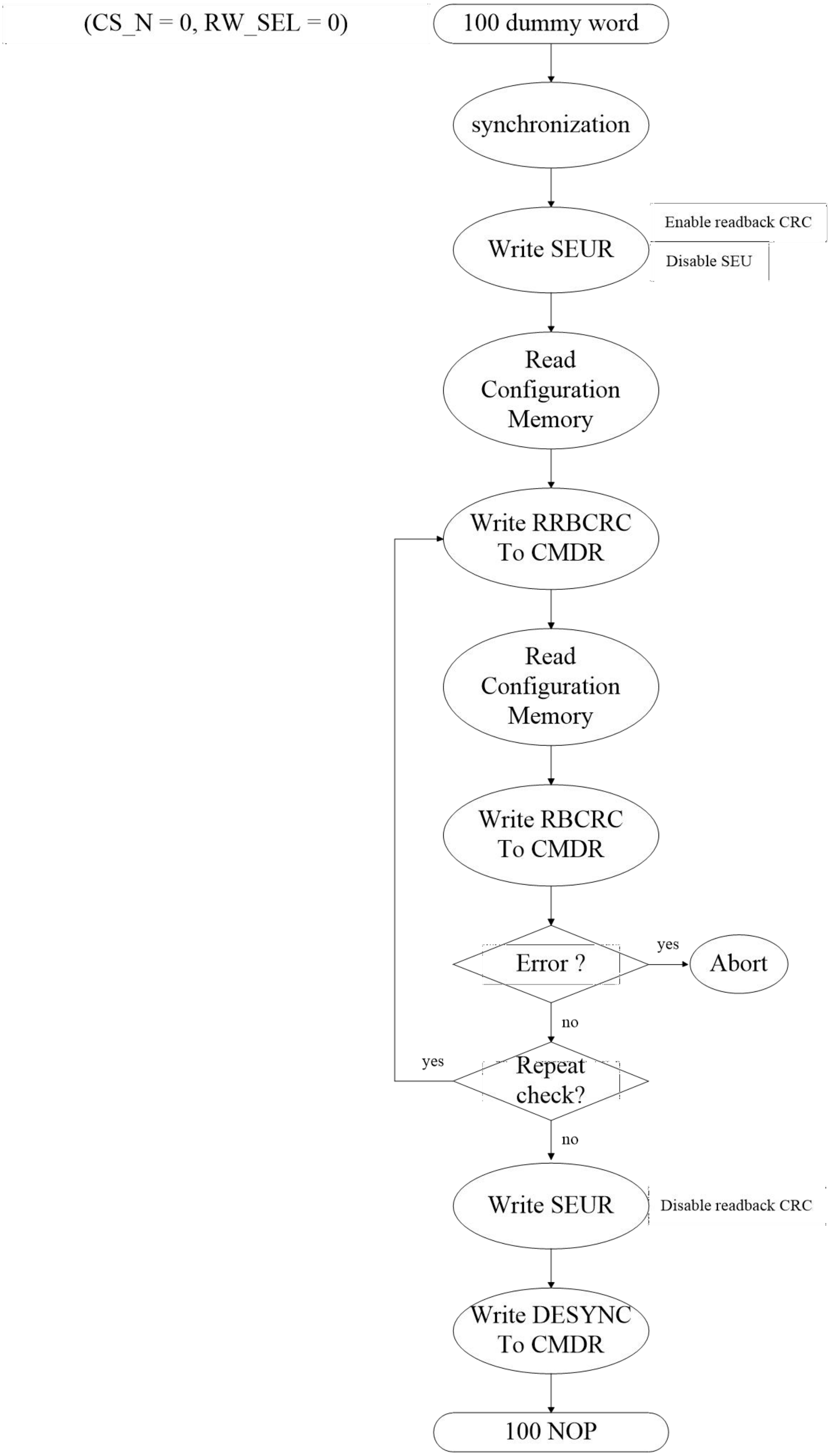


Figure 2 Read back CRC flow chart

2.3 SEU Check process

SEU error detection supports two types of single-step operation and continuous operation. The specific processes of the two operations are now introduced in detail.

Table 2 SEU single-step inspection process

100 fill words (32'hFFFFFFFF) bit stream
Synchronize
1 Write the SEU register to disable reading back the CRC and enable SEU error detection and correction.
2 Read back frame 1: 100 fill words (32'hFFFFFFFF) sync words Type 1 packet header: no operation to write ADRR register Write RCMEM command to CMDR register Write the header of the type 1 packet, used to read the CMEMOR register. Write the header of the type 2 packet, used to read the data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register Write NOP command to CMDR register
3 View SEU results No errors: proceed to step 4 Single bit/double bit error: proceed to step 6
4 If all frame error detection and correction are completed, then proceed to step 7, otherwise proceed to step 5
5 Read back the next frame: Write ADRR register Write RCMEM command to CMDR register Write the header of the type 1 packet, used to read the CMEMOR register. Write the header of the type 2 packet, used to read the data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register Write NOP command to CMDR register Proceed to step 3

6 Dynamic reconfiguration of the current frame: Write the RSTCRC command to the CMDR register. Write the DRCFGEN command to the CMDR register. Write the VDDTDOWN command to the CMDR register. Empty header (wait 4us) Write ADRR register Write WCMEM command to CMDR register Write the header of type 1 packet, used to write the CMEMIR register. Write the header of type 2 packet, used to write data. Write to CMEMIR register Write the WCMEMDIS command to the CMDR register. Write the VDDTUP command to the CMDR register. Write CRCR register Write the DRCFGDIS command to the empty header of the CMDR register (wait 4us) Check the dynamic reconfiguration results and proceed to step 4 .
7 Write the SEU register, disable reading back CRC, and disable SEU error detection and correction.
8 Write DESYNC command to CMDR register
9 100 no-op type 1 headers

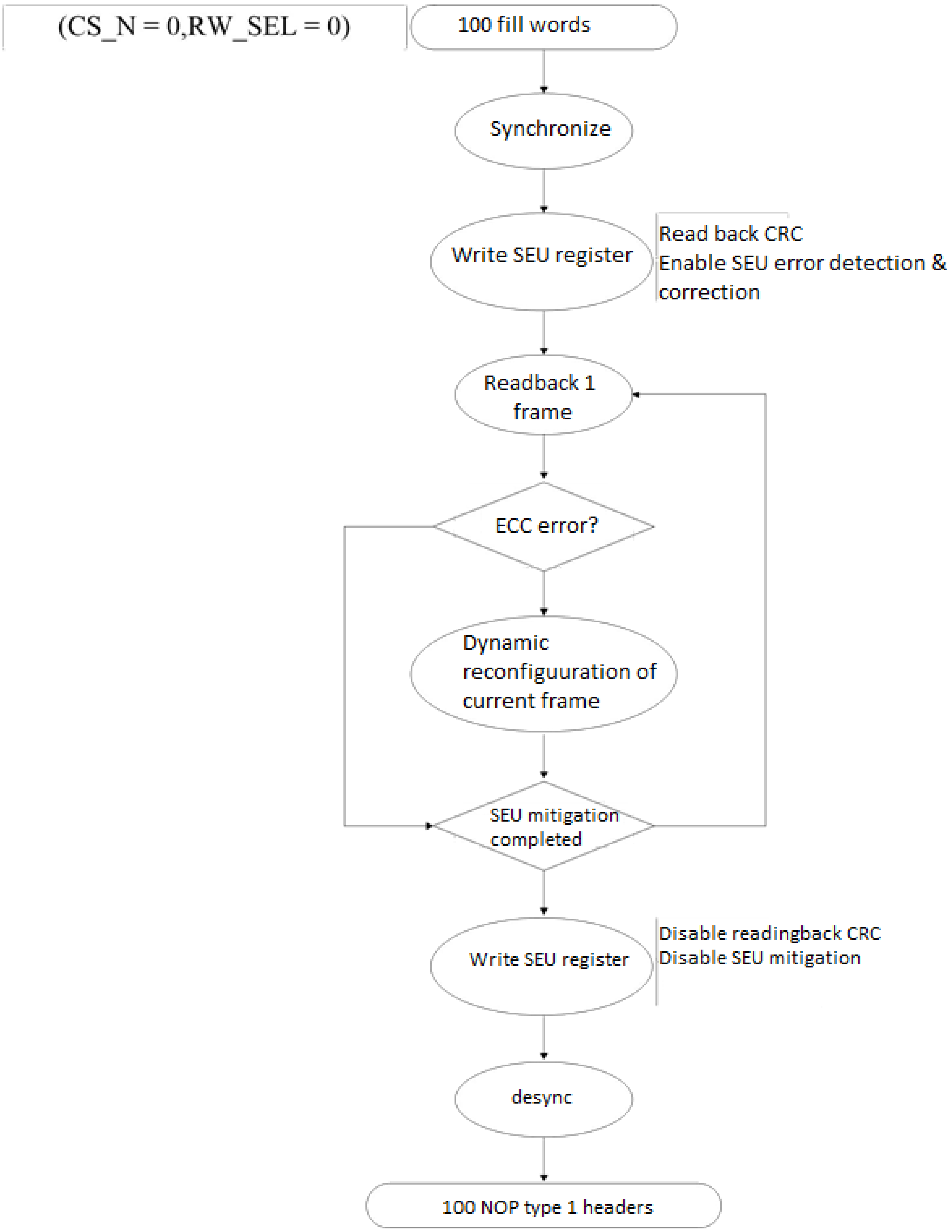


Figure 3 SEU single-step detection flow chart

The following describes the continuous SEU detection process:

Table 3 SEU continuous testing flow chart

100 fill words (32'hFFFFFFFF)
Synchronize
1 Write the SEU register to disable CRC readback and enable SEU error mitigation.

2 Starting from frame 1, read back all non-DRM frames in the configuration memory: 100 fill words (32'hFFFFFFFF) sync words Type 1 packet header: no operation Write ADRR register (1st frame) Write RCMEM command to CMDR register Write the header of the type 1 packet, used to read the CMEMOR register Write the header of the type 2 packet for reading data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register. Write the NOP command to the CMDR register. View SEU results Write ADRR register (2nd frame) Write RCMEM command to CMDR register Write the header of the type 1 packet, used to read the CMEMOR register. Write the header of the type 2 packet, used to read the data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register. Write the NOP command to the CMDR register. View SEU results … Write ADRR register (last frame) Write RCMEM command to CMDR register Write the header of the type 1 packet, used to read the CMEMOR register. Write the header of the type 2 packet, used to read the data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register. Write the NOP command to the CMDR register. View the SEU results (the next frame address is 0)
3 Read back a single-bit error frame: Write ADRR register Write RCMEM command to CMDR register

Write the header of the type 1 packet, used to read the CMEMOR register. Write the header of the type 2 packet, used to read the data. Wait at least 40 clock cycles (CS_N is 1, clock CLK continues) to read the CMEMOR register Write the RCMEMDIS command to the CMDR register. Write the NOP command to the CMDR register. View SEU results
4 Dynamic reconfiguration of the current frame: Write the RSTCRC command to the CMDR register. Write the DRCFGEN command to the CMDR register. Write the VDDTDOWN command to the CMDR register. Empty header (wait 4us) Write ADRR register Write WCMEM command to CMDR register Write the header of type 1 packet, used to write the CMEMIR register. Write the header of type 2 packet, used to write data. Write to CMEMIR register Write the WCMEMDIS command to the CMDR register. Write the VDDTUP command to the CMDR register. Write CRCR register Write the DRCFGDIS command to the empty header of the CMDR register (wait 4us) View dynamic reconfiguration results
5 If all single-bit error frame corrections are not completed, proceed to step 3 If all single-bit error frames are corrected, proceed to step 6

6 Dynamic reconfiguration of all double-bit error frames: Write the RSTCRC command to the CMDR register. Write the DRCFGEN command to the CMDR register. Write the VDDTDOWN command to the CMDR register. Empty header (wait 4us) Write the ADRR register (the first double-bit error frame) and write the WCMEM command to the CMDR register Write the header of the type 1 packet, used to write the CMEMIR register Write the header of the type 2 packet, used to write data (if multiple double-bit error frame addresses are consecutive, they can be written together in one operation) Write to CMEMIR register Write WCMEMDIS command to CMDR register Write the ADRR register (2nd double-bit error frame) and write the WCMEM command to the CMDR register Write the header of type 1 packet, used to write the CMEMIR register. Write the header of type 2 packet, used to write data. Write to CMEMIR register Write WCMEMDIS command to CMDR register ... Write the ADRR register (the last double-bit error frame) and write the WCMEM command to the CMDR register Write the header of type 1 packet, used to write the CMEMIR register. Write the header of type 2 packet, used to write data. Write to CMEMIR register Write the WCMEMDIS command to the CMDR register. Write the VDDTUP command to the CMDR register. Write CRCR register Write the DRCFGDIS command to the empty header of the CMDR register (wait 4us) View dynamic reconfiguration results
7 Write the SEU register, disable reading back CRC, and disable SEU error detection and correction.
8 Write DESYNC command to CMDR register
9 100 no-op type 1 headers

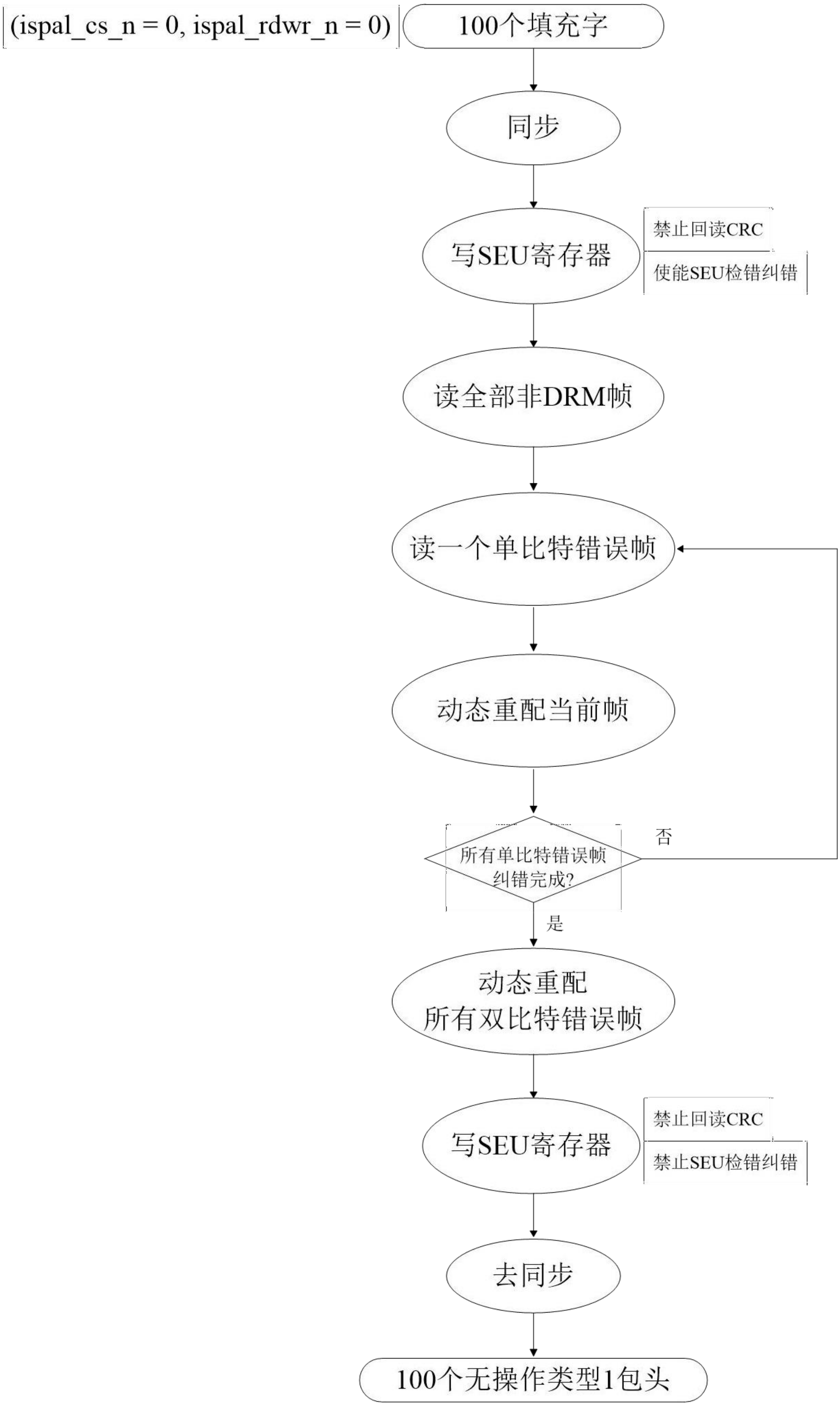


Figure 4 SEU continuous detection flow chart

2.4 GTP_IPAL_E2 port list

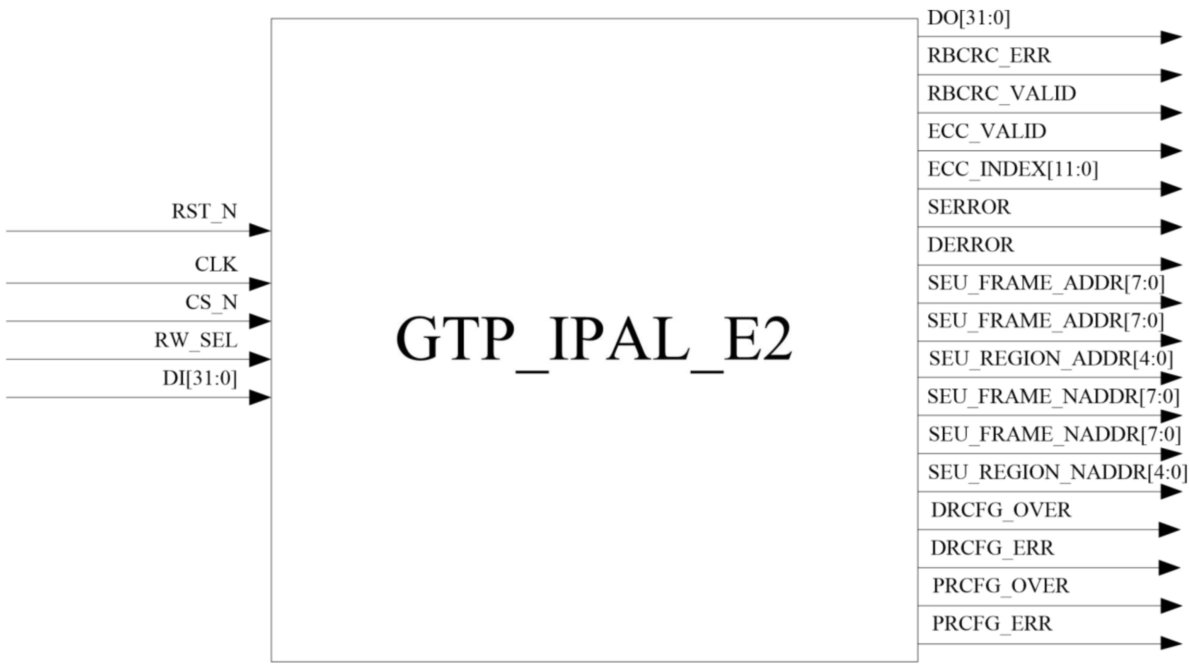


Figure 5 GTP_IPAL_E2 port diagram

GTP_IPAL_E2 has 5 input ports, 17 output ports, and 2 parameters. Instructions or data can be input through the DI port to read and write the corresponding configuration register, or to write and read back the data of a certain frame in a certain column of a certain area in the configuration memory. CRC detection or SEU detection can be performed on the data read back.

Table 4 GTP_IPAL_E2 interface list

SIGNAL NAME	I/O	BIT WIDTH	DESCRIPTION
GLOBAL SIGNAL			
CLK	I	1	Internal parallel interface clock
RST_N	I	1	Reset signal, active low level
IPAL INTERFACE			
CS_N	I	1	Chip select signal, active low level
RW_SEL	I	1	Read and write options: 0 for writing, 1 for reading;
DI	I	32	data input
DO	O	32	data output
READ BACK CRC INTERFACE			
RBCRC_ERR	O	1	Read back CRC error flag, active high.
RBCRC_VALID	O	1	Read back the CRC valid flag, valid high, lasting 1 clock cycle.
SEU READBACK INTERFACE			

ECC_VALID	O	1	ECC valid flag, high valid.
ECC_INDEX	O	12	Address index for single bit error
SERROR	O	1	Single bit error flag detected by SEU
DERROR	O	1	Double-bit error flag detected by SEU
SEU_FRAME_ADDR	O	8	Current frame address detected by SEU
SEU_COLUMN_ADDR	O	8	Current column address detected by SEU
SEU_REGION_ADDR	O	5	Current zone address detected by SEU
SEU_FRAME_NADDR	O	8	Next frame address detected by SEU
SEU_COLUMN_NADDR	O	8	The next column address detected by SEU
SEU_REGION_NADDR	O	5	Next area address detected by SEU
PRCFG_OVER	O	1	Partial reconfiguration completion flag. When it is 1 , it indicates that the partial reconfiguration is completed.
PRCFG_ERR	O	1	Partial reconfiguration error flag, indicating the partial reconfiguration result when PRCFG_OVER is valid.
DRCFG_OVER	O	1	Dynamic reconfiguration end flag. When it is 1 , it indicates that dynamic reconfiguration is completed.
DRCFG_ERR	O	1	Dynamic reconfiguration error flag, indicating the dynamic reconfiguration result when DRCFG_OVER is valid.

2.5 Parameter definition

Table 5 GTP_IPAL_E2 parameters

PARAMETER	DESCRIPTION
IDCODE	Device IDCODE , default value 32'haaaa5555
DATA_WIDTH	Parallel data bit width, configure the GTP parallel port data bit width through CCS. Please refer to CCS configuration for details.

2.6 Interface timing

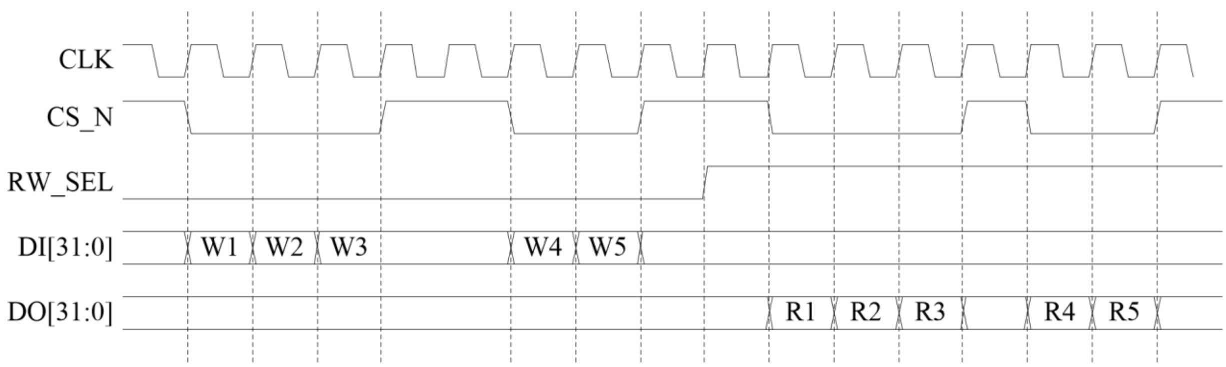


Figure 6 GTP_IPAL_E2 read and write interface timing

Note: The RW_SEL signal transition can only occur when CS_N is high.

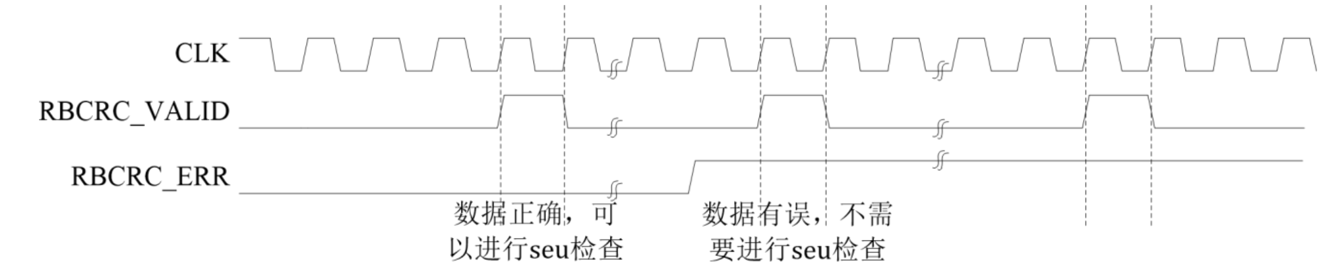


Figure 7 CRC readback sampling valid data timing

CRC readback status RBCRC _ERR status is sampled when RBCRC_VALID is valid. RBCRC_VALID is a pulse signal maintained for 1 clock cycle.

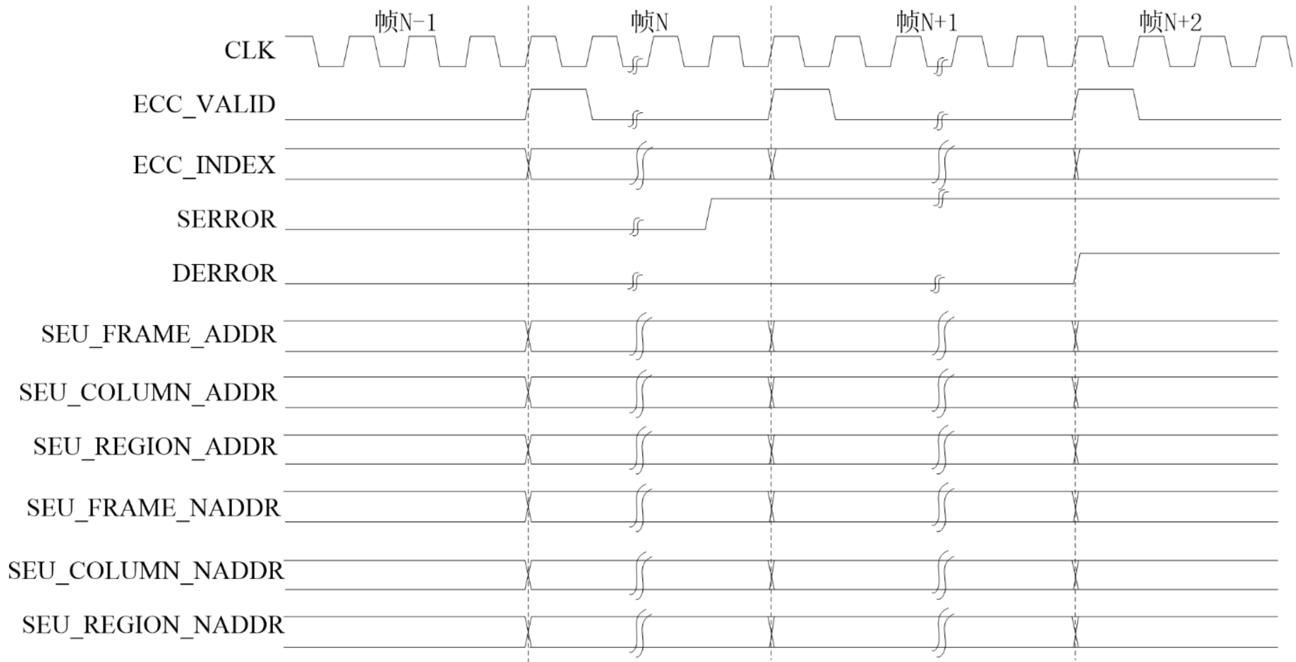


Figure 8 ECC readback sampling valid data timing

When the signal ECC_VALID is valid, the SEU-related detection status and signal value are valid.

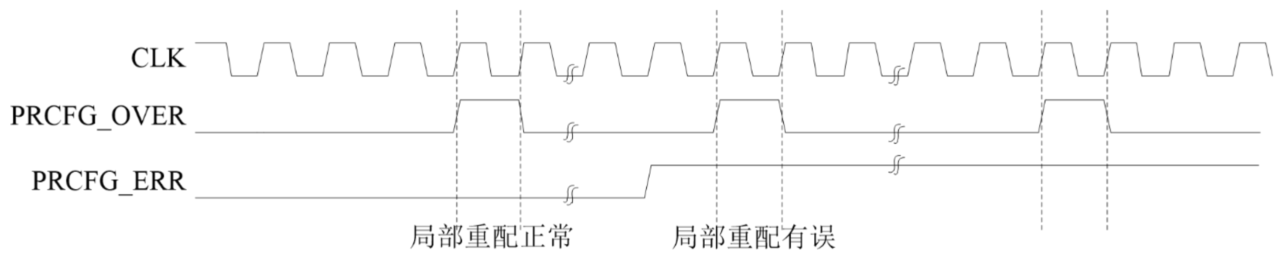


Figure 9 Local configuration status readback sampling valid data timing

When PRCFG_OVER is high, the PRCFG_ERR value is valid.

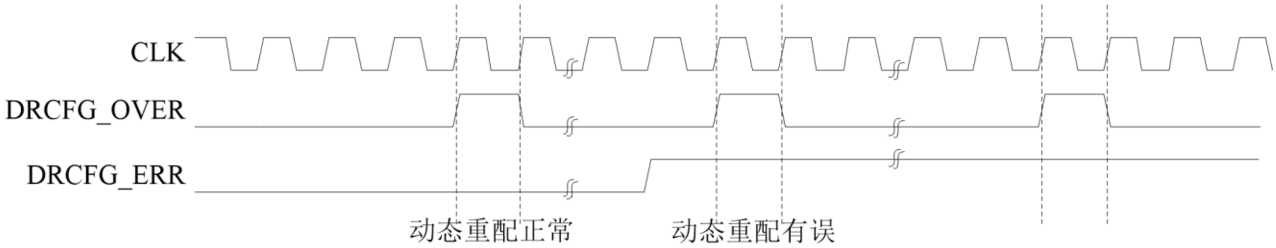


Figure 10 Dynamic configuration status readback sampling valid data timing

When DRCFG_OVER is high, the DRCFG_ERR value is valid.

2.7 Register description

The registers used by the SEU detection module are as follows. For detailed explanation, please refer to the corresponding description of CCS .

Table 6 SEU detection related registers

Name	R/W	Address	Description
CRCR	R/W	00000	CRC register
CMDR	R/W	00010	command register
CMEMIR	W	00101	Frame data input register
CMEMOR	R	00111	Frame data output register
STATUSR	R	01001	status register
ADRR	R/W	01011	frame address register
SEUR	R/W	01101	SEU control register
SEUSTATUSR	R	01110	SEU status register
OPTION1R	R/W	11010	option register 1
SEUADDR	R	11101	SEU frame address register
SEUNADDR	R	11111	SEU lower frame address register

3. Reference design

TBC

3.1 Reference functional design

(Reference design function introduction, functional block diagram, main module introduction, etc.)

none.

3.2 Reference Design Interface List

(Reference design interface definition)

none.

3.3 Reference design file directory

(Refer to the file directory definition used by the design delivery customer)

none.

3.4 Reference design simulation

(Reference design simulation design, introduction to simulation platform, brief introduction to each module, how to run, etc.; if simulation cannot be provided for individual designs, delete this part)

none.

3.5 Reference design on-board verification

(Board verification method, verification process, verification results, data, etc...)

none.